PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H04S 1/00	A1	(11) International Publication Number: WO 98/36614 (43) International Publication Date: 20 August 1998 (20.08.98)

(21) International Application Number: PCT/IB98/00073

(22) International Filing Date: 19 January 1998 (19.01.98)

(30) Priority Data:
08/800,636 14 February 1997 (14.02.97) US

(71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(71) Applicant *(for SE only)*: PHILIPS NORDEN AB [SE/SE]; Kottbygatan 7, Kista, S-164 85 Stockholm (SE).

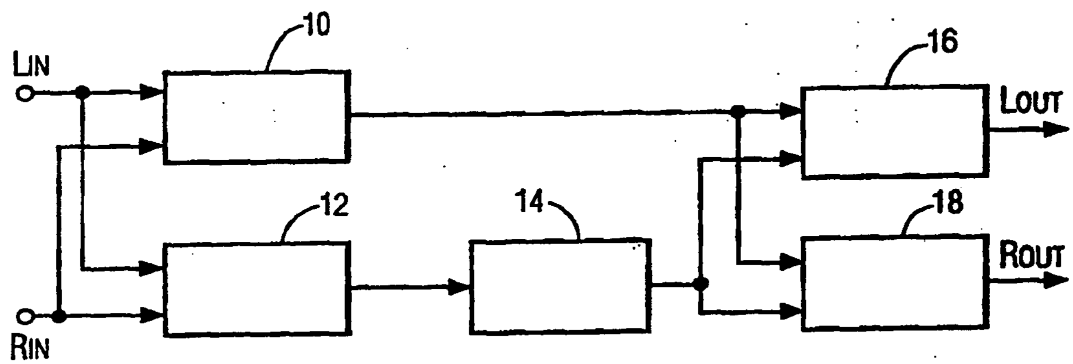
(72) Inventor: SCHOTT, Wayne, M.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agent: GROENENDAAL, Antonius, W., M.; Internationaal Octrooibureau B.V., P.O. Box 220, NL-5600 AE Eindhoven (NL).

(81) Designated States: JP, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: CREATING AN EXPANDED STEREO IMAGE USING PHASE SHIFTING CIRCUITRY



(57) Abstract

In portable stereo radio receivers and television receivers, the loudspeakers therein may be separated only by a limited amount. This severely restricts the stereo image created by the loudspeakers. A circuit arrangement for creating an expanded stereo image may be incorporated in such receivers. This circuit arrangement first forms a combined monaural signal (at 10) and a differential signal (at 12) from the two stereo signals (L_{in}, R_{in}). The differential signal is then subjected to a phase shift (at 14). The phase-shifted differential signal is then matrixed (at 16, 18) with the combined monaural signal to form output stereo signals (L_{out}, R_{out}). When reproduced through stereo loudspeakers, the stereo image appears to be greatly expanded, beyond the limited placement of the loudspeakers.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	**ES**	Spain	**LS**	Lesotho	**SI**	Slovenia
AM	Armenia	**FI**	Finland	**LT**	Lithuania	**SK**	Slovakia
AT	Austria	**FR**	France	**LU**	Luxembourg	**SN**	Senegal
AU	Australia	**GA**	Gabon	**LV**	Latvia	**SZ**	Swaziland
AZ	Azerbaijan	**GB**	United Kingdom	**MC**	Monaco	**TD**	Chad
BA	Bosnia and Herzegovina	**GE**	Georgia	**MD**	Republic of Moldova	**TG**	Togo
BB	Barbados	**GH**	Ghana	**MG**	Madagascar	**TJ**	Tajikistan
BE	Belgium	**GN**	Guinea	**MK**	The former Yugoslav Republic of Macedonia	**TM**	Turkmenistan
BF	Burkina Faso	**GR**	Greece			**TR**	Turkey
BG	Bulgaria	**HU**	Hungary	**ML**	Mali	**TT**	Trinidad and Tobago
BJ	Benin	**IE**	Ireland	**MN**	Mongolia	**UA**	Ukraine
BR	Brazil	**IL**	Israel	**MR**	Mauritania	**UG**	Uganda
BY	Belarus	**IS**	Iceland	**MW**	Malawi	**US**	United States of America
CA	Canada	**IT**	Italy	**MX**	Mexico	**UZ**	Uzbekistan
CF	Central African Republic	**JP**	Japan	**NE**	Niger	**VN**	Viet Nam
CG	Congo	**KE**	Kenya	**NL**	Netherlands	**YU**	Yugoslavia
CH	Switzerland	**KG**	Kyrgyzstan	**NO**	Norway	**ZW**	Zimbabwe
CI	Côte d'Ivoire	**KP**	Democratic People's Republic of Korea	**NZ**	New Zealand		
CM	Cameroon			**PL**	Poland		
CN	China	**KR**	Republic of Korea	**PT**	Portugal		
CU	Cuba	**KZ**	Kazakstan	**RO**	Romania		
CZ	Czech Republic	**LC**	Saint Lucia	**RU**	Russian Federation		
DE	Germany	**LI**	Liechtenstein	**SD**	Sudan		
DK	Denmark	**LK**	Sri Lanka	**SE**	Sweden		
EE	Estonia	**LR**	Liberia	**SG**	Singapore		

Creating an expanded stereo image using phase shifting circuitry

Background of the invention

Field of The Invention

The subject invention relates to a signal processing circuit for enhancing a stereo image that corresponds to a stereo audio signal.

Description of The Related Art

In conventional stereo systems, the amplifying circuits amplify the left and right channel signals and pass these amplified signals to a left and right channel loudspeakers. This is done in an attempt to simulate the experience of a live performance in which the reproduced sounds emanate from different locations. Since the advent of stereo systems, there has been continual development of systems which more closely simulate this experience of a live performance. For example, in the early to mid 1970's, four-channel stereo systems were developed which included two front left and right channel loudspeakers and two rear left and right channel speakers. These systems attempted to recapture the information contained in signals reflected from the back of a room in which a live performance was being held. More recently, surround sound systems are currently on the market which, in effect, seek to accomplish the same effect.

A drawback of these systems is that there are four or more channels of signals being generated and a person must first purchase the additional loudspeakers and then solve the problem of locating the multiple loudspeakers for the system.

As an alternative to such a system, U.S. Patent 4,748,669 to Klayman discloses a stereo enhancement system which simulates this wide dispersal of sound while only using the two stereo loudspeakers. This system, commonly known as the Sound Retrieval System, uses dynamic equalizers, which boost the signal level of quieter components in the audio spectrum relative to louder components, a spectrum analyzer and a feedback and reverberation control circuit to achieve the desired effect. However, as should be apparent, this system is relatively complex and costly to implement.

Summary of the invention

It is an object of the present invention to provide a circuit arrangement for enhancing the imaging of a stereo signal such that it seems much larger than the actual spacing between the stereo loudspeakers.

It is a further object of the invention to provide such a circuit arrangement that is relatively simple and inexpensive to implement.

The above objects are achieved in a circuit arrangement for creating an expanded stereo image in a stereo signal, comprising a first input and a second input for receiving, respectively, a left channel signal and a right channel signal of in input stereo signal; first combining means coupled to the first and second inputs for additively combining the left and right channel signals thereby forming a sum signal; first difference forming means also coupled to the first and second inputs for forming a difference between the left and right channel signals, thereby forming a difference signal; phase shifting means having an input for receiving said difference signal; second difference forming means having a first input for receiving said sum signal and a second input coupled to an output of said phase shifting means, said second difference forming means forming a left channel output signal; and second summing means having a first input for receiving said sum signal and a second input coupled to the output of said phase shifting means, said second summing means forming a right channel output signal.

Applicant has found that in small portable stereo receivers and in television receivers, the spacing between the stereo loudspeakers is limited. When the circuit arrangement of the subject invention is incorporated in such receivers, the stereo image is greatly expanded, much beyond the limited placement of the stereo loudspeakers.

Brief description of the drawings

With the above and additional objects and advantages in mind as will hereinafter appear, the invention will be described with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram of a circuit arrangement for a first embodiment of the invention;

Fig. 2 is a block diagram of a modified circuit arrangement for a second embodiment of the invention;

Fig. 3 shows a plot of the response curves of the left output signal and the left crosstalk signal for the circuit arrangement of Fig. 2;

Fig. 4 shows a plot of the response curve of a phase shifter arrangement in the circuit arrangement of Fig. 2;

Fig. 5 shows a plot of response curves for the circuit arrangement of Fig. 2; and

Fig. 6 is a schematic diagram of the circuit arrangement for the second embodiment of the invention of Fig. 2.

Description of the preferred embodiments

Fig. 1 shows a basic block diagram of a circuit arrangement forming a first embodiment of the invention. A left channel input signal is applied to an input LIN of the circuit arrangement and then to a first input of a first summing circuit 10. A right channel input signal is applied to an input RIN of the circuit arrangement and then to a second input of the first summing circuit 10. Similarly, the left and right channel input signals are applied to first and second inputs, respectively, of a first difference circuit 12. An output from the first difference circuit 12 is applied to a phase shifter 14. An output from the first summing circuit 10 is connected to first inputs of a second difference circuit 16 and a second summing circuit 18,respectively, while an output from the phase shifter 14 is connected to second inputs of the second difference circuit 16 and the second summing circuit 18, respectively. The output LOUT of the second difference circuit 16 supplies the left channel output signal, while the output ROUT of the second summing circuit 18 supplies the right channel output signal.

The first summing circuit 10 is used to generate a monaural signal (L+R) and the first difference circuit 12 is used to generate a differential signal (L-R). This is done to prevent amplitude and phase fluctuations in the left and right channel output signals when the circuit arrangement is driven by an (L+R) signal.

The circuit arrangement as shown in Fig. 1 does indeed produce the desired expansion of the stereo image when the gains in the summing and difference circuits are not balanced.

Fig. 2 shows a basic block diagram of a working embodiment of the invention. In particular, the left channel input signal is applied to an input LIN of the circuit arrangement, while the right channel input signal is applied to an input RIN. The input LIN is connected to the first inputs of a first matrix circuit 20 and a second matrix circuit 22, respectively, and the input RIN is connected to the second input of the first and second matrix circuits 20 and 22, respectively. The first matrix circuit 20 forms the sum signal (L+R) and has a gain of 0 dB. The second matrix circuit 22 forms the difference signal (L-R) and has a gain of 14 dB. the output from the second matrix circuit 22 is applied to a phase shifter arrangement 24. The output from the first matrix circuit 20 is applied to the first inputs of a third matrix circuit 26 and a fourth matrix circuit 28, while the output from the phase shifter arrangement 24 is applied to the second

inputs of the third and fourth matrix circuits 26 and 28. The third matrix circuit 26, which supplies the left channel output signal to the output LOUT of the circuit arrangement, provides a 0 dB gain for the output from the first matrix circuit 20, and a 6 dB gain for the output from the phase shifter arrangement 24. The fourth matrix circuit 28, which supplies the right channel output signal to the output ROUT of the circuit arrangement, provides a 0 dB gain for the output signal from the first matrix circuit 20, and a 6 dB gain for the output signal from the phase shifter arrangement 24.

The phase shifter arrangement 24 is formed by the series arrangement of two all pass phase shifters 30 and 32, each providing a gain of -6 dB. As such, the net gain for the (L+R) signal is 0 dB, while the net gain for the (L-R) signal is 8 dB, such that in certain areas of the audio frequency range, the differential between the desired left or right signal and the corresponding right or left cross-talk signal is 7-8 dB. This is shown in the plots A and B of Fig. 3, in which the responses of the LOUT signal and the ROUT cross-talk signal, respectively, are shown with respect to frequency. Fig. 3 further shows plots C and D of the phase of the LOUT signal and the ROUT crosstalk signal with respect to frequency.

Fig. 4 shows a plot of the amplitude response/gain E (in dB) with respect to frequency, and the combined phase F (in degrees) with respect to frequency of the phase shifter arrangement 24. It should be noted that the amplitude response/gain produces a flat line at -12 dB, while the phase varies from approximately -60 degrees to -700 degrees.

Fig. 5 shows a plot of the overall gain (in dB) and phase (in degrees) of the circuit arrangement. In Fig. 5, line G represents the (L+R) gain, line H represents the (L+R) phase response, line I represents the amplitude response of a single channel (L or R), and line J represents the phase response of a single channel (L or R).

Fig. 6 is a schematic diagram of circuit arrangement for a practical embodiment of the invention. In particular, the left input LIN is connected to ground through a resistor R1 and, through the series arrangement of a first capacitor C1, a second capacitor C2 and a resistor R2 to the inverting input of a differential amplifier A1. Similarly, the right input RIN is connected to ground through a resistor R1 and, through the series arrangement of a capacitor C3 and a resistor R4, to the inverting input of summing amplifier A2. The junction between capacitors C1 and C2 is also connected to the inverting input of summing amplifier A2 through a resistor R5, while the junction between capacitor C3 and resistor R4 is connected to the non-inverting input of differential amplifier A1 through the series combination of capacitor C4 and resistor R6. The inverting input of summing amplifier A2 is connected to its output via a resistor R7. Arranged as

such, differential amplifier A1 forms the matrix circuit 22 while summing amplifier A2 forms the matrix circuit 20.

The inverting input of differential amplifier A1 is connected to its output through a resistor R8 which is then connected, on the one hand, through a resistor R9, to the non-inverting input of differential amplifier A3, and on the other hand, through the series combination of a resistor R10 and a capacitor C5, to the inverting input of differential amplifier A3. The non-inverting input of differential amplifier A1 is also connected to ground through resistor R11, as is the non-inverting input of differential amplifier A3 connected to ground through resistor R12. The junction between resistor R10 and capacitor C5 is connected to the output of differential amplifier A3 via a capacitor C6, while the inverting input of differential amplifier A3 is connected to its output via a resistor R13.

The output of differential amplifier A3 is connected, on the one hand, through the series arrangement of a resistor R14 and a capacitor C7, to the inverting input of differential amplifier A4, and, on the other hand, through a resistor R15, to the non-inverting input of differential amplifier A4. The non-inverting input of differential amplifier A4 is connected to ground via resistor R16. The junction between resistor R14 and capacitor C7 is connected to the output of differential amplifier A4 via a capacitor C8, while the inverting input of differential amplifier A4 is connected to its output via a resistor R17. Differential amplifiers A3 and A4 thus form phase shifters 30 and 32 of the phase shifter arrangement 24.

The output of differential amplifier A4 is connected to the non-inverting input of differential amplifier A5, while the output of differential amplifier A2 is connected to the inverting input of differential amplifier A5 via a resistor R18. A resistor R19 connects the inverting input of differential amplifier A5 with its output which is, in turn, connected, through a series arrangement of a capacitor C9 and a resistor R20, to ground, the junction between the capacitor C9 and resistor R20 being connected to the left output LOUT. As such, differential amplifier A5 forms the matrix circuit 26.

The output of differential amplifier A2 is connected to the inverting input of differential amplifier A6 via a resistor R21, while the output of differential amplifier A4 is connected to this inverting input via a resistor R22. The non-inverting inputs of differential amplifiers A2 and A6 are connected to ground. A resistor R23 connects the non-inverting input of differential amplifier A6 to its output which is, in turn, connected, through the series combination of a capacitor C10 and a resistor R24, to ground, the junction between capacitor

C10 and resistor R24 being connected to the right output ROUT. As such, differential amplifier A6 forms the matrix circuit 28.

In an exemplary embodiment, the values of the above components are as follows:

RESISTORS

R1, R3, R20, R24	100 KΩ
R2, R6, R7, R18, R19, R22	10 KΩ
R4, R5, R21, R23	20 KΩ
R8, R11	27 KΩ
R9, R12, R15, R16	47 KΩ
R10, R14	8.2 KΩ
R13, R17	33 KΩ

CAPACITORS

C1, C3, C9, C10	5 μF
C2, C4	0.1 μF
C5, C6	47 nF
C7, C8	6.8 nF

The differential amplifiers A1-A6 are each type LF347.

Numerous alterations and modifications of the structure herein disclosed will present themselves to those skilled in the art. However, it is to be understood that the above described embodiment is for purposes of illustration only and not to be construed as a limitation of the invention. All such modifications which do not depart from the spirit of the invention are intended to be included within the scope of the appended claims.

CLAIMS

1. A circuit arrangement for creating an expanded stereo image in a stereo signal, comprising:

a first input and a second input for receiving, respectively, a left channel signal and a right channel signal of in input stereo signal;

first combining means coupled to the first and second inputs for additively combining the left and right channel signals thereby forming a sum signal;

first difference forming means also coupled to the first and second inputs for forming a difference between the left and right channel signals, thereby forming a difference signal;

phase shifting means having an input for receiving said difference signal; second difference forming means having a first input for receiving said sum signal and a second input coupled to an output of said phase shifting means, said second difference forming means forming a left channel output signal; and

second summing means having a first input for receiving said sum signal and a second input coupled to the output of said phase shifting means, said second summing means forming a right channel output signal.

2. A circuit arrangement as claimed in claim 1, wherein said first and second combining means each comprises a matrix circuit.

3. A circuit arrangement as claimed in claim 2, wherein said first and second difference forming means each comprises a matrix circuit.

4. A circuit arrangement as claimed in claim 3, wherein said first combining means has a gain of 0 dB; said second combining means has a gain of 0 dB for the signal from the first combining means, and a gain of 6 dB for the signal from the phase shifting means; said first difference forming means has a gain of 14 dB; said second difference forming means has a gain of 0 dB for the signal from the first combining means, and a gain of 6 dB for the signal from the phase shifting means; and the phase shifting means has a gain of -12 dB.

5. A circuit arrangement as claimed in claim 1, wherein said phase shifting means comprises a series arrangement of two phase shifters, each of said phase shifters being all-pass (0E - 360E) phase shifting networks.

6. A circuit arrangement as claimed in claim 4, wherein said phase shifting means comprises a series arrangement of two phase shifters, each of said phase shifters being an all-pass (0E - 360E) phase shifting network having a gain of -6 dB.

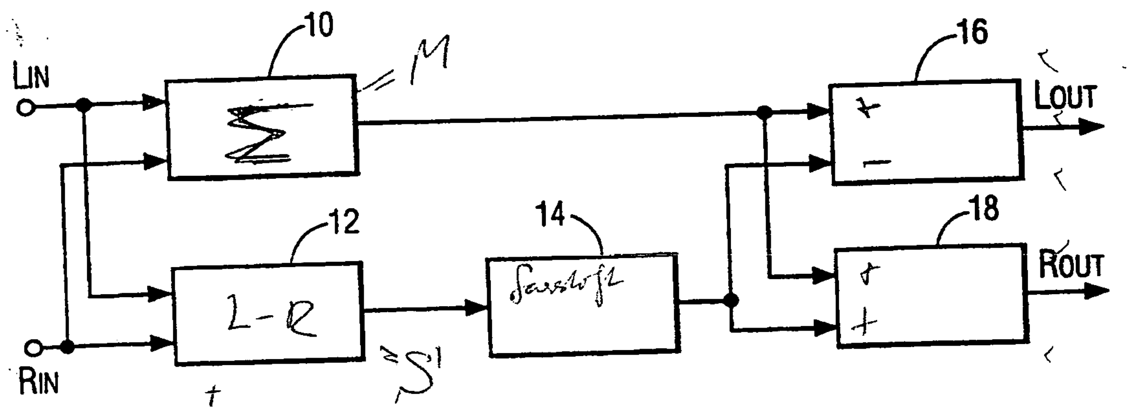

10
16
LIN
LOUT
12
14
18
ROUT
L-R
RIN

FIG. 1

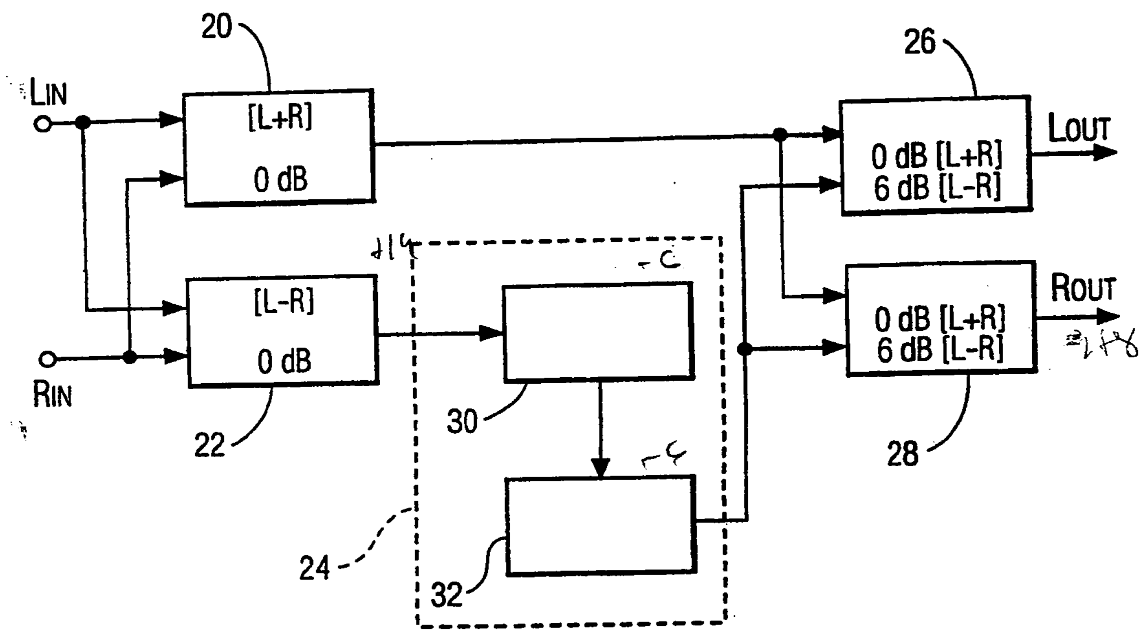

20
26
LIN
[L+R]
0 dB
LOUT
0 dB [L+R]
6 dB [L-R]
[L-R]
0 dB
ROUT
0 dB [L+R]
6 dB [L-R]
RIN
30
22
28
24
32

FIG. 2

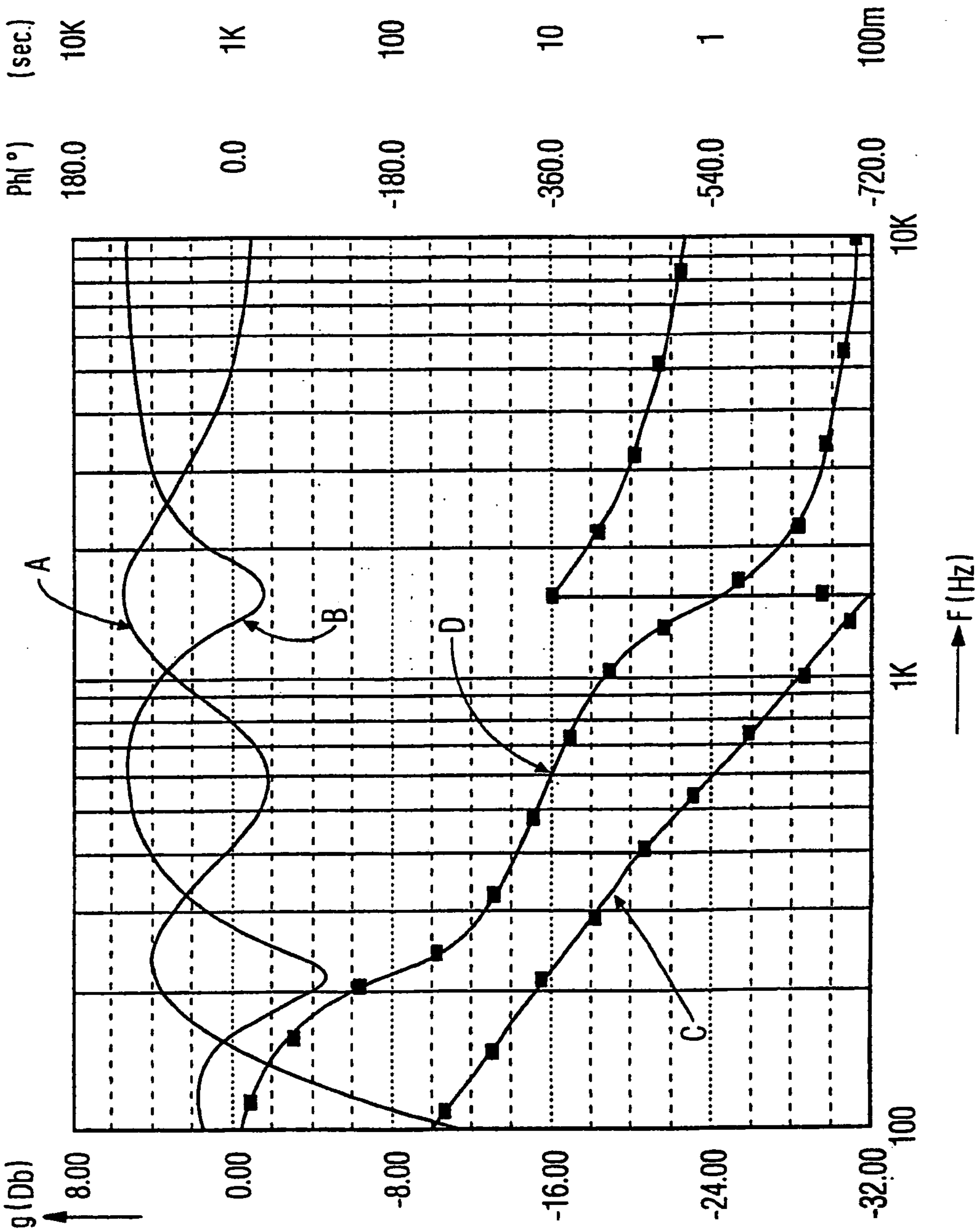

g (Db)
8.00
0.00
-8.00
-16.00
-24.00
-32.00
100
1K
10K
F (Hz)
Ph(°)
180.0
0.0
-180.0
-360.0
-540.0
-720.0
Del. (sec.)
10K
1K
100
10
1
100m
A
B
C
D

FIG. 3

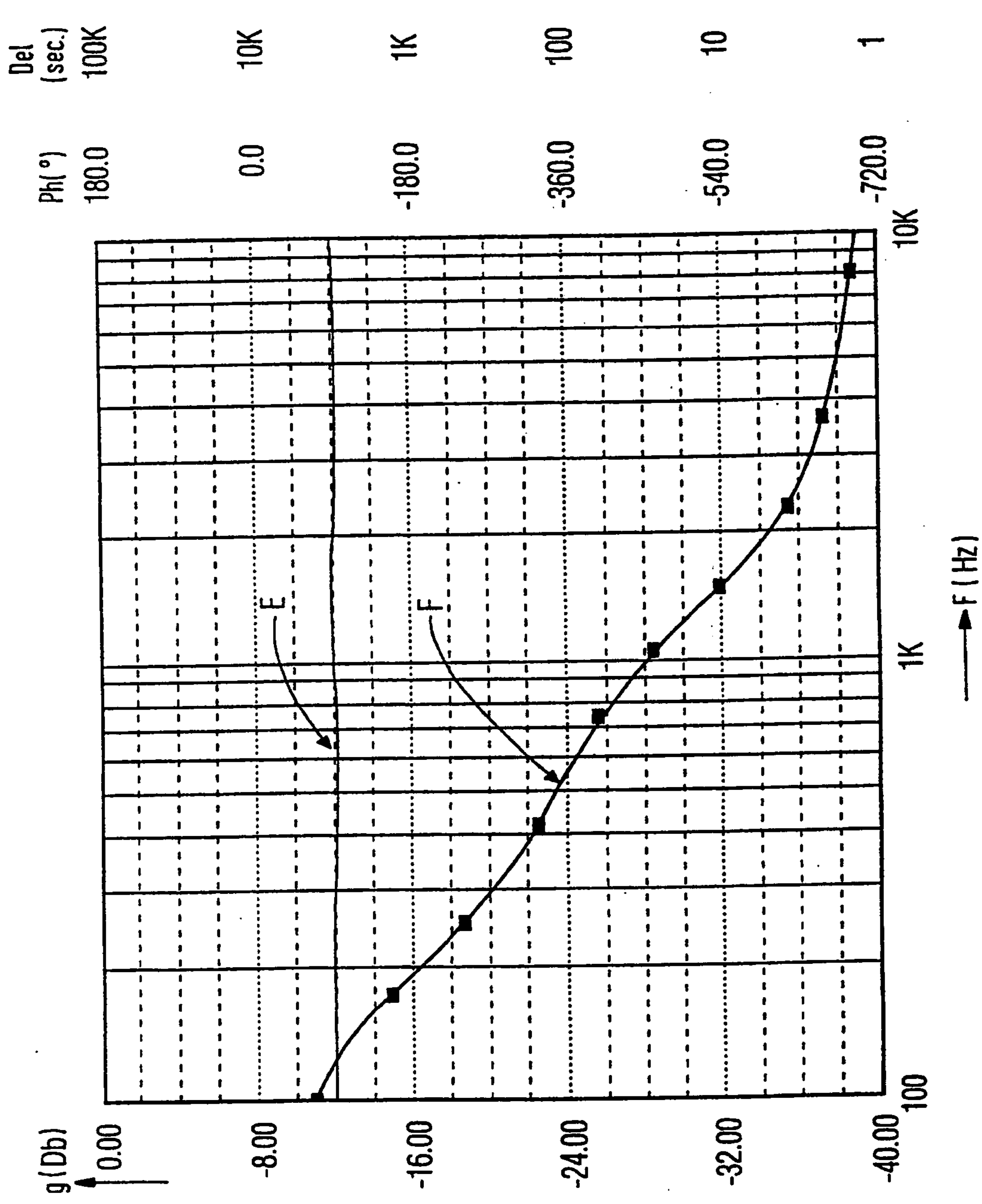

g (Db)
0.00
-8.00
-16.00
-24.00
-32.00
-40.00
100
1K
10K
F (Hz)
Ph(°)
180.0
0.0
-180.0
-360.0
-540.0
-720.0
Del
(sec.)
100K
10K
1K
100
10
1
E
F

FIG. 4

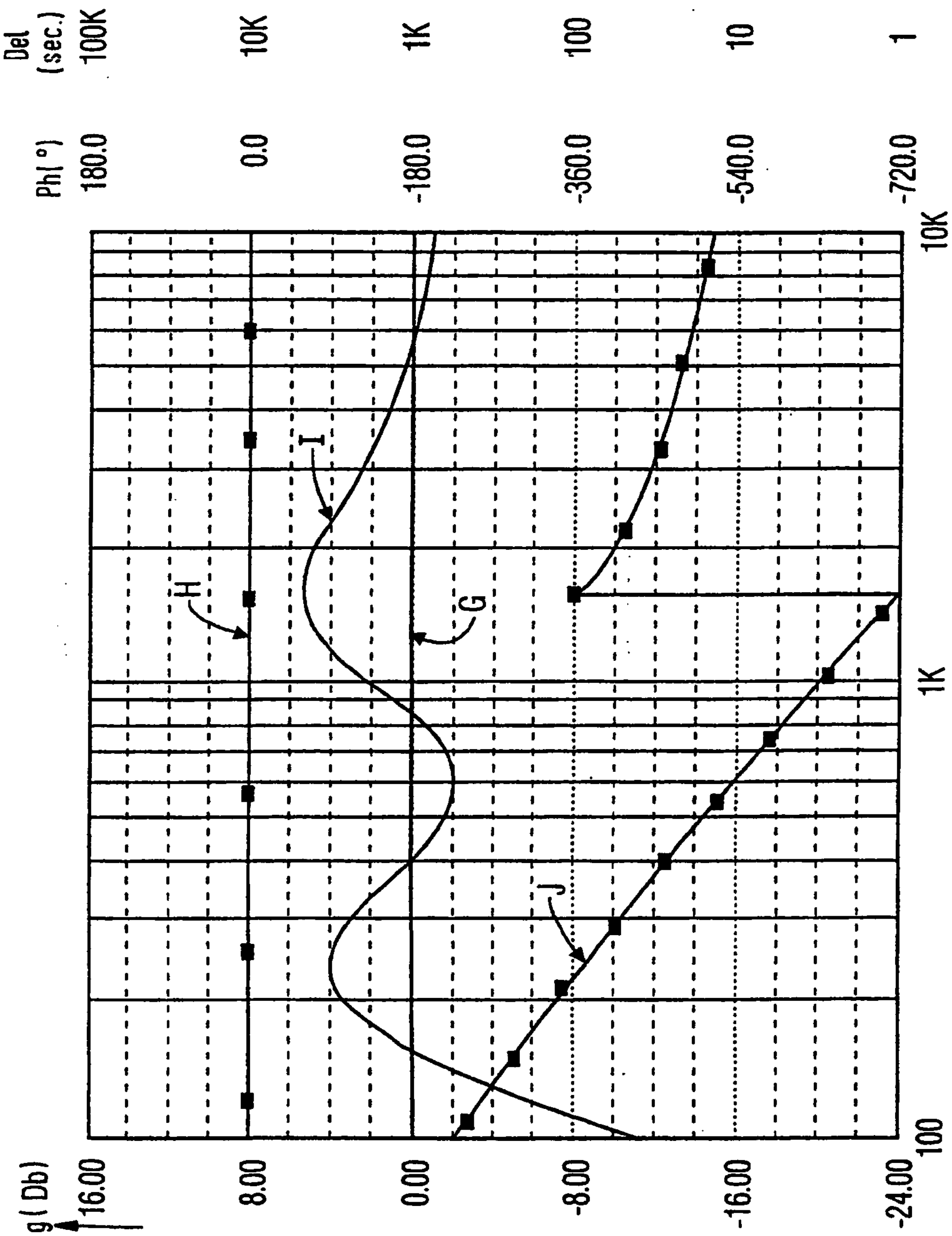

g(Db)
16.00
8.00
0.00
-8.00
-16.00
-24.00
Ph(°)
180.0
0.0
-180.0
-360.0
-540.0
-720.0
Del (sec.)
100K
10K
1K
100
10
1
100
1K
10K
F(Hz)
H
I
G
J

FIG. 5

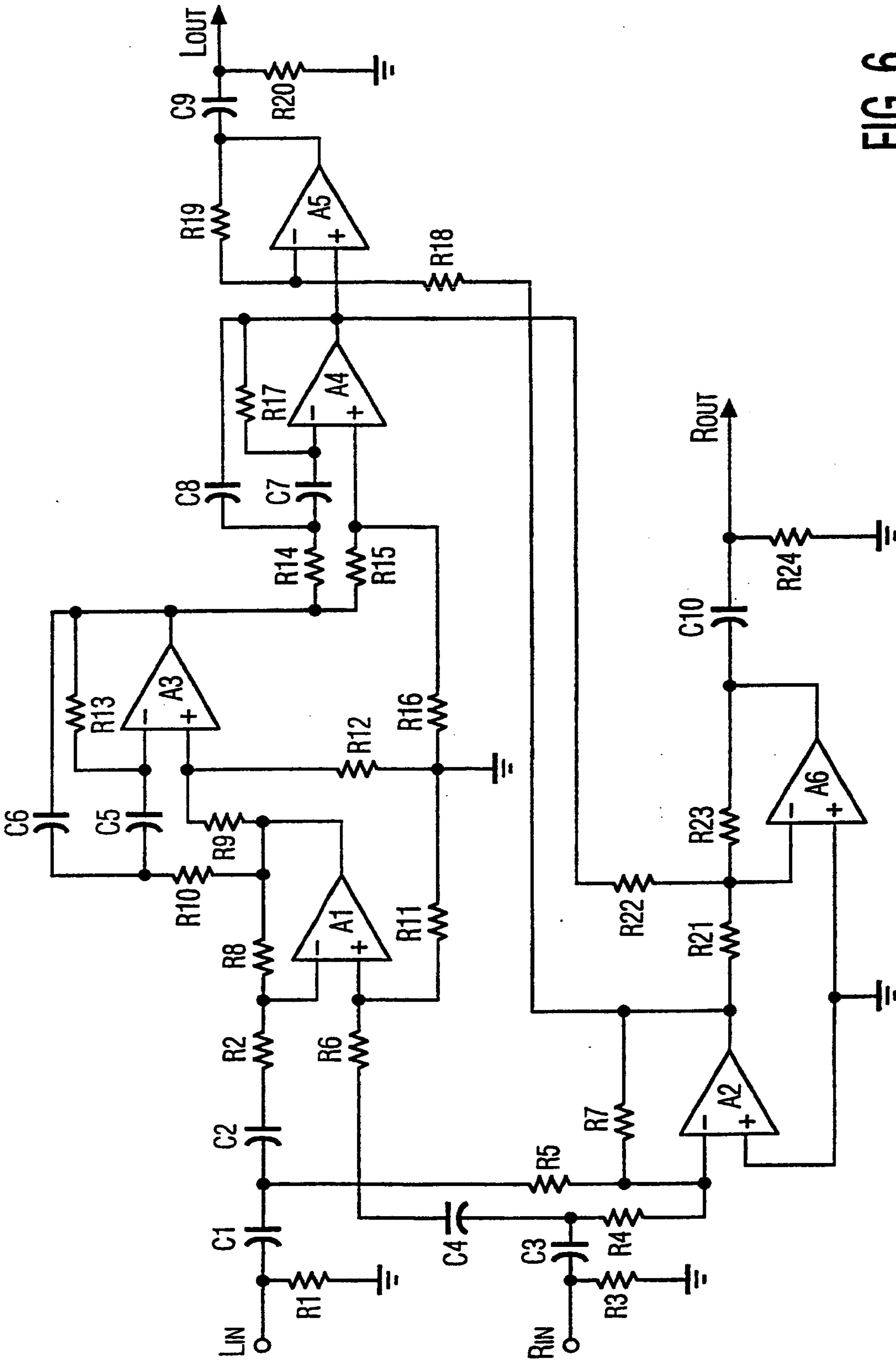

LOUT
ROUT
LIN
RIN
A1
A2
A3
A4
A5
A6
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB 98/00073

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H04S 1/00
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H04R, H04S

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPODOC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4451927 A (D.L. HERSHBERGER), 29 May 1984 (29.05.84) --	1-3
A	US 4349698 A (M. IWAHARA), 14 Sept 1982 (14.09.82) --	
A	US 4748669 A (A.I. KLAYMAN), 31 May 1988 (31.05.88) --	
A	US 4841572 A (A.I. KLAYMAN), 20 June 1989 (20.06.89) -- --------	

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" erlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 June 1998	24 -06- 1998
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Leif Vingård Telephone No. +46 8 782 25 00

INTERNATIONAL SEARCH REPORT
Information on patent family members

29/04/98

International application No.
PCT/IB 98/00073

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4451927 A	29/05/84	NONE	
US 4349698 A	14/09/82	JP 1254855 C	12/03/85
		JP 56001698 A	09/01/81
		JP 59031279 B	01/08/84
US 4748669 A	31/05/88	AU 587529 B	17/08/89
		AU 591609 B	07/12/89
		AU 597848 B	07/06/90
		AU 2205288 A	08/12/88
		AU 2205388 A	08/12/88
		AU 6934187 A	20/10/87
		CA 1284297 A	21/05/91
		DE 3752025 D,T	12/06/97
		DE 3752034 D,T	30/10/97
		DE 3752052 D,T	07/08/97
		DE 3784423 A,T	08/04/93
		EP 0262160 A,B	06/04/88
		SE 0262160 T3	
		EP 0476790 A,B	25/03/92
		SE 0476790 T3	
		EP 0478096 A,B	01/04/92
		SE 0478096 T3	
		EP 0479395 A,B	08/04/92
		SE 0479395 T3	
		EP 0748143 A	11/12/96
		HK 75293 A	06/08/93
		JP 2528154 B	28/08/96
		JP 2609065 B	14/05/97
		JP 7007798 A	10/01/95
		JP 7007799 A	10/01/95
		JP 63502945 T	27/10/88
		WO 8706090 A	08/10/87
US 4841572 A	20/06/89	CA 1299111 A	21/04/92
		KR 9402166 B	18/03/94
		WO 9011670 A	04/10/90